Interfaces in Computing, 2 (1984) 249 - 258

ANALOGUE-TO-DIGITAL AND DIGITAL-TO-ANALOGUE 12-BIT INTERFACES FOR DIRECT DIGITAL CONTROL USING AN AIM-65 MICROCOMPUTER

CHARLES CAPADAY and JULES O'SHEA

Electrical Engineering Department, Ecole Polytechnique de Montréal, Montreal, Quebec H3C 3A7 (Canada)

(Received February 7, 1984)

Summary

In this paper the design and operation of an analogue-to-digital (A/D) converter and a digital-to-analogue (D/A) converter interfaced to an AIM-65 8-bit microcomputer are described. These converters are built from integrated circuits on two separate printed-circuit cards. The A/D card also incorporates an eight-channel multiplexer, and the D/A card has a latch that keeps the output constant while the data acquisition takes place.

1. Introduction

In this paper the design of 12-bit analogue-to-digital (A/D) and digital-to-analogue (D/A) converters interfaced to an 8-bit AIM-65 microcomputer is described. The assembly language subroutines controlling the converters are also described. The design objective was the development of a system which is inexpensive yet complete and of adequate performance. This system was intended for research work on the control of robot manipulators and for teaching our undergraduate students the principles of the digital control of dynamic systems. It was thus important to keep the cost low so as to be able to reproduce the prototype many times. Before the design details of the A/D and D/A converters could be decided, we had to choose a microcomputer suitable for our purposes. The AIM-65 microcomputer was chosen for the following reasons. Briefly, for about U.S. $600 a system based on the popular 6502 microprocessor can be obtained which includes a 20-character light-emitting diode display and a 20-character thermal printer, an editor, an assembler, a BASIC interpreter, a cassette interface, two 8-bit bidirectional ports PA and PB and a programmable real-time clock. The last two characteristics are implemented in the 6522 integrated circuit (IC) known as the versatile interface adapter (VIA). This microprocessor support chip is very well suited to input–output (I/O) intensive real-time applications such as direct digital control. In particular this IC allows 12-bit converters to be

0252-7308/84/$3.00

easily interfaced to 8-bit microcomputers (the 6500 and 6000 series) and thus eases the limitations mentioned in ref. 1. The resolution of the converter is an important point noteworthy of some discussion. Typically, quality control systems such as position servo systems provide a resolution of some 0.1%. Clearly, 8-bit converters (1/246) cannot provide such resolution, whereas 12-bit converters (1/4096) easily accommodate this requirement.

The choice of the particular 12-bit A/D and D/A converter system remained. Most of the commercially available systems are intended for large applications, are costly and often require additional purchases of hardware such as motherboards (STD-Bus, Multibus etc.) for interfacing to a microcomputer. It was thus decided to design and build our own 12-bit A/D and D/A converter system using commercially available ICs. The costs and the implementation time to produce a complete system compare favourably with the costs of purchasing commercially available systems.

In Section 2 the interconnections between the AIM-65 and the converter cards are described. In Section 3, each card is described in detail. This is followed in Section 4 by a description of the assembly language subroutines controlling the A/D and the D/A converters.

2. Configuration of the interface

The A/D and D/A converters, together with their respective support ICs, were each mounted on a 6.25 in × 4.5 in printed-circuit card. Both of these cards were connected in parallel to the AIM-65's J1 application connector via a 22-pin edge connector (Fig. 1). Thus both cards share the same I/O ports. Such a parallel interconnection was made possible by using a three-state A/D converter. Thus, during operation of the D/A converter the 12 output pins of the A/D converter are placed in the high Z state.

Of the 22 pins necessary for the interconnection between the AIM-65 and the converter cards, 12 are used for I/O (*i.e.* either for outputting a word to the D/A converter or for reading the converted value from the A/D converter). These pins correspond to the VIA pins PB0 - PB7 and the pins PA0, PA1, PA2 and PA7. Three pins are used for selecting one of eight pos-

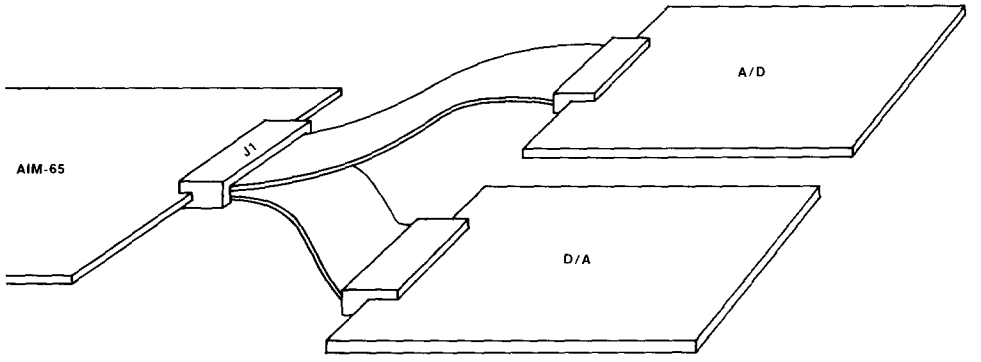


Fig. 1. Connection of the A/D and D/A cards to the AIM-65.

sible input channels (X0 - X7) to the A/D converter; these are the VIA pins PA4, PA5 and PA6. Four pins CA1, CA2, CB2 and PA3 are used for control-and-status purposes to be described shortly. Finally, one pin (pin 1) is used as the common ground (GND). The various categories (I/O, multiplex, control and status) of interconnection described are highlighted in Figs. 2 and 4.

2.1. The analogue-to-digital converter card

The layout of the A/D converter card is shown in Fig. 2. The "heart" of the circuit is the AD 574 A/D converter. The DG 508 multiplexer is used to select, via software, one of eight possible input channels (X0 - X7) to the A/D converter. Each of these eight input channels is preceded by an operational amplifier (μA 741) which not only serves for impedance matching but also with some simple modifications can be used to filter the input signals. It should be noted that our design did not include any sample-and-hold circuit between the multiplexer and the converter. This was done to simplify the design and for ease of operation as well as to reduce production costs. The bandwidth of the signals (0 - 15 Hz) in our applications was so small compared with the conversion time (35 μs maximum) that such sample-and-hold circuits were not needed. In fact, since the A/D converter operates by successive approximations and the signal has little variation during the conversion interval, the least significant bits are fixed at the end of this interval and thus reflect the signal amplitude at that moment whereas, if a zero-order hold were used, the least significant bits would represent the signal amplitude at the beginning of the conversion interval. Thus the time at which the least significant bits are set in these two methods differs by only 35 μs (maximum).

The high slew rate buffer amplifier LM 310 [3] between the output of the multiplexer and the input to the A/D converter was chosen because the sum of the slewing and settling times of the buffer amplifier must be shorter than the time between channel switching and the start of conversion. Otherwise, the converter would convert some of the transient output of the amplifier.

The AD 574 converter requires five control signals for operation. However, with a particular application in mind, certain choices were made definitively. Thus the 12/8 pin (Fig. 2) was wired high (+5 V) and the A0 pin low (GND), thereby selecting the 12-bit output. The sequence of controls chosen is shown in the chronogram in Fig. 3. This was the simplest mode that allowed both activation of the converter and subsequent placing of its 12 output pins in the high Z state. Briefly, just before conversion, the chip enable pin CE is brought high, and conversion is initiated when the read and convert pin R/C is brought low and then high again (a negative pulse of not more than 1 μs). The end of conversion (data ready) is indicated on the status pin STS; this signal goes high just after the start conversion pulse and then low again to indicate end of conversion (data ready). Thus a simple handshake sequence was established.

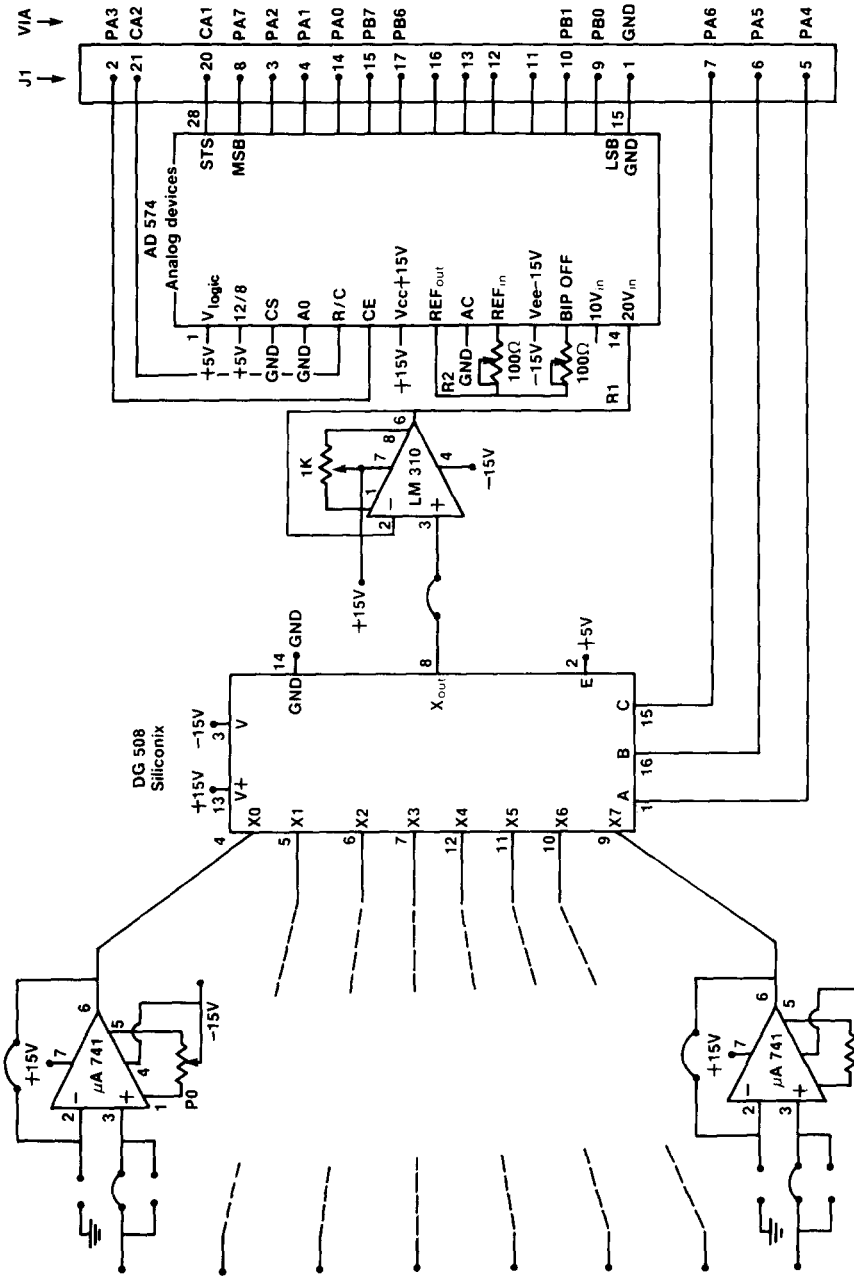


Fig. 2. Schematic diagram of the A/D board: LSB, least significant bit; MSB, most significant bit. For further details relative to the AD 574, see ref. 2.

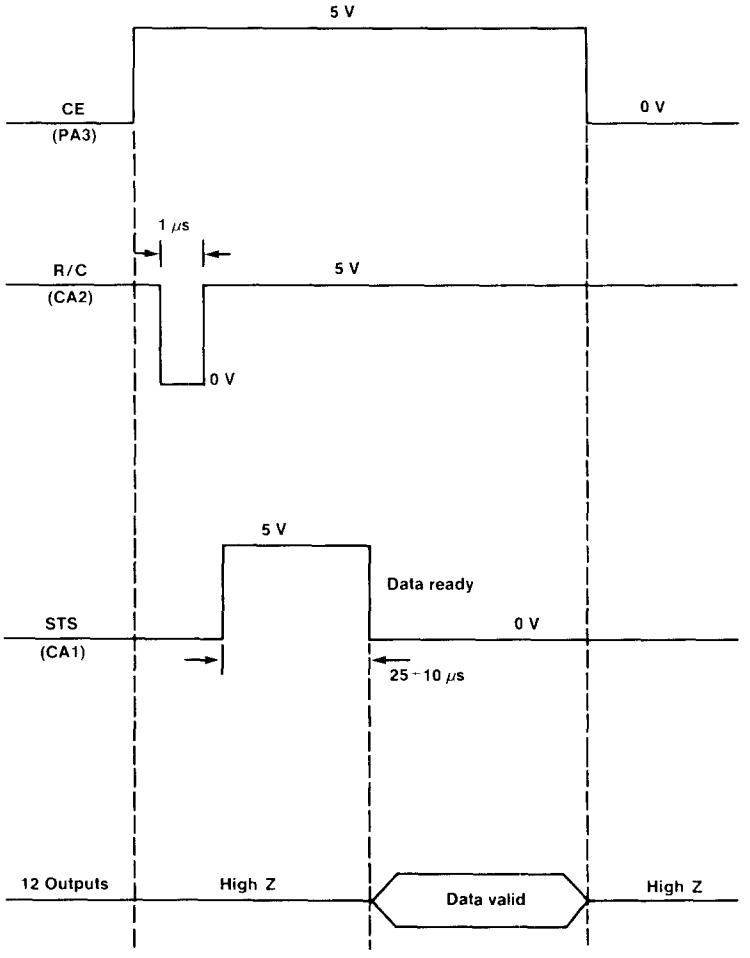


Fig. 3. Chronogram of the A/D conversion sequence.

Using the A/D converter in the 20 V span gives a resolution of

$$\frac{\Delta V}{\text{bit}} = \frac{20\ \text{V}}{2^{12}} = 4.88\ \text{mV bit}^{-1}$$

The 12-bit binary word b at the output of the converter is related to the input voltage V_{in} by

$$b = B\left\{Q\left(\frac{V_{in} + 10}{20} \times 2^{12}\right)\right\} \tag{1}$$

where Q is the quantification operator giving the largest whole number in the argument and B is the operator transforming this decimal number into a binary number.

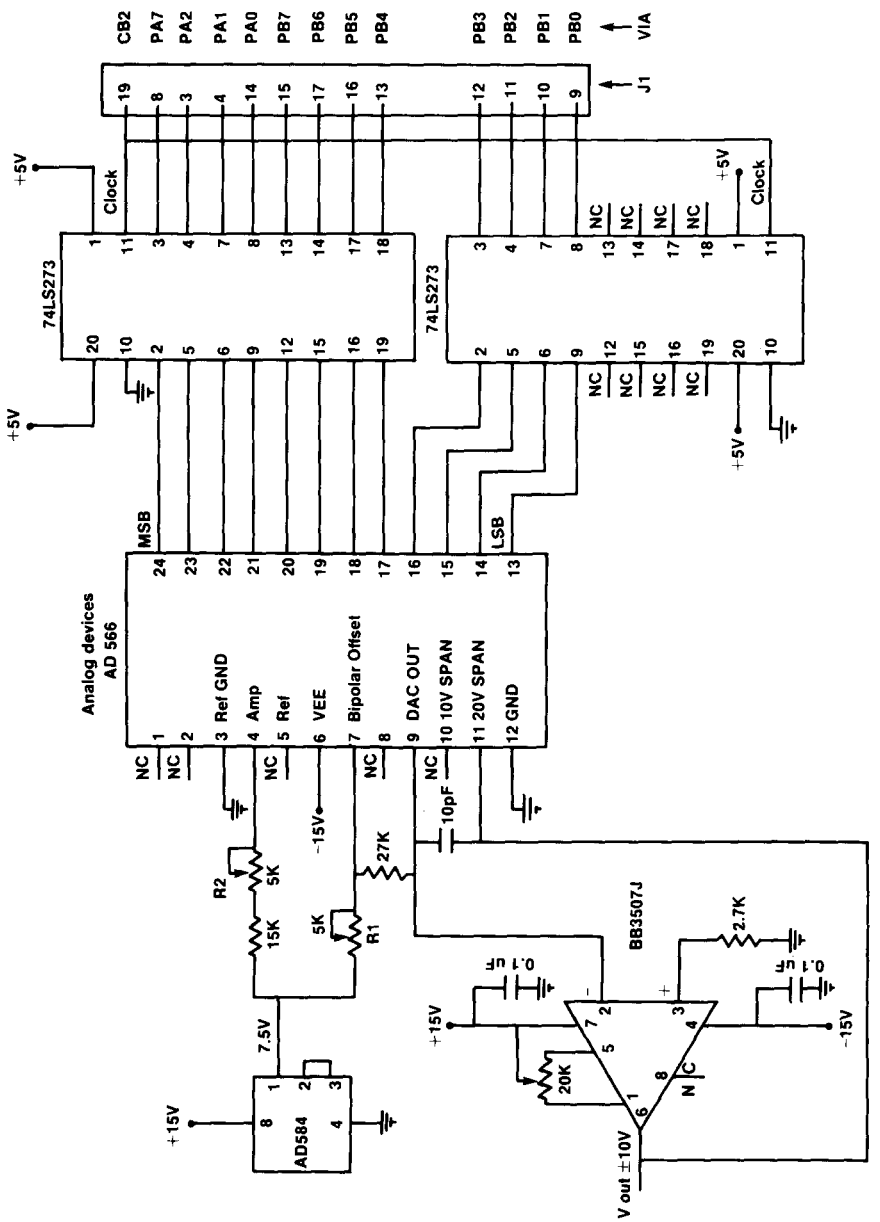


Fig. 4. Schematic diagram of the D/A converter card: NC, not connected. For further details relative to the AD 566, see ref. 2.

2.2. The digital-to-analogue converter card

The layout of the D/A converter card is shown in Fig. 4. Since the AIM-65's J1 application connector serves both the A/D and the D/A converters, a means of latching the 12-bit input word to the D/A converter during operation of the A/D converter (the sampling period) was needed. This was done by putting D-type flip-flops 74LS273 before the input pins to the D/A converter. In addition to the data latches and the AD 566 converter, the card contains a precision voltage reference source, the AD 584, used in conjunction with the D/A IC and a fast slewing buffer amplifier BB3507J [4] connected to the output of the converter.

The operation of this card is very simple. A positive-going (0 - 5 V) signal on the clock pin CK of the D-type flip-flops will latch the input word from the D input to the G output. The latching is controlled through the CB2 pin of the VIA. Once the output word appears at the input pins of the converter, it is converted to a voltage in about 25 + 10 ns. This output voltage remains constant as long as the output word is kept on the input pins. Using the D/A converter in the −10 V to +10 V span, the output voltage V_{out} is related to the input word by the equation

$$V_{out} = \frac{20B^{-1}(b)}{2^{12}} - 10 \tag{2}$$

where b is the binary number to be converted and B^{-1} is the operator transforming a binary number into a decimal number.

3. Conversion subroutines

For completeness and immediate utility to interested readers, the assembly (6502) language subroutines used to control the converters are described. As an introduction, let us recall the necessary control-and-status signals required for operation of the converters. The A/D converter requires the chip enable and the start conversion signals. It returns a data ready signal. This sequence must be preceded by selection of an input channel to the converter via the multiplexer. The D/A converter is considerably simpler to operate as it requires only a positive-going signal on the CK pin of the data latches. These requirements, in each case, plus the requirements particular to the VIA operations [5] naturally lead to the microprocessor instructions.

3.1. The analogue-to-digital conversion subroutine

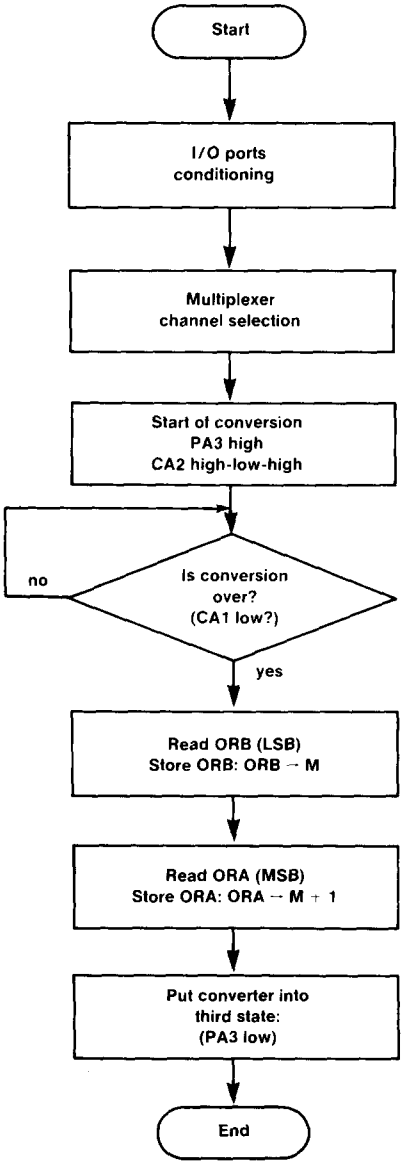
The sequence of operations necessary for A/D conversion is summarized in the flow chart shown in Fig. 5(a); the actual subroutine is listed in Fig. 5(b). The sequence is as follows.

(1) The I/O ports are appropriately designated as either inputs or outputs.

(2) The input channel is selected.

(3) The converter is activated (A3 high; CA2 negative pulse not less than 1 μs).

(4) The end of conversion is determined by polling, *i.e.* by querying whether CA1 has gone low.



(a)

```
Ø233 A9 LDA #ØØ
Ø235 8D STA AØØ2
Ø238 A9 LDA #78
Ø23A 8D STA AØØ3
Ø23D A9 LDA #18
Ø23F 8D STA AØØ1
Ø242 A9 LDA #ØE
Ø244 8D STA AØØC
Ø247 A9 LDA #ØC
Ø249 8D STA AØØC
Ø24C A9 LDA #ØE
Ø24E 8D STA AØØC
Ø251 AD LDA AØØD
Ø254 29 AND #Ø2
Ø256 FØ BEQ Ø251
Ø258 AD LDA AØØ1
Ø25B 29 AND #87
Ø25D 85 STA Ø3
Ø25F AD LDA AØØØ
Ø262 85 STA Ø2
Ø264 A9 LDA #ØØ
Ø266 8D STA AØØ1
```

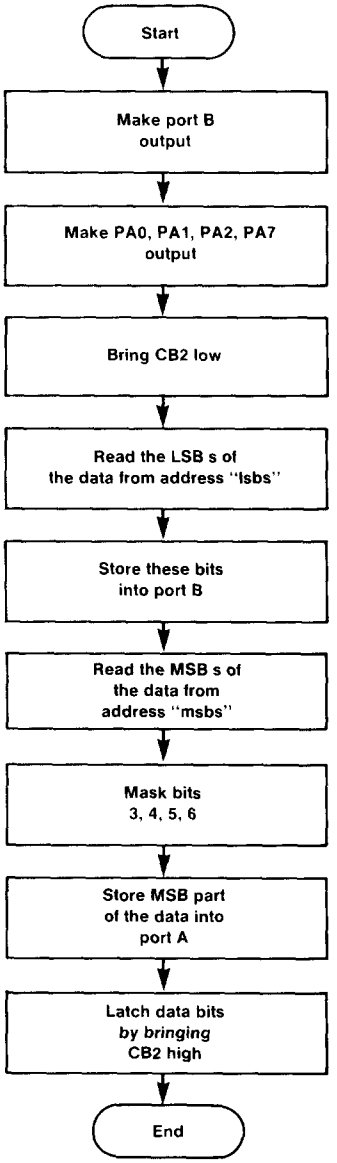
(b)

Fig. 5. (a) A/D subroutine flow chart and (b) A/D subroutine listing: ORB, output register B; ORA, output register A.

(5) When conversion is completed, the output register B is read into memory M, thus storing the least significant bits.

(6) The output register A is read into memory M + 1, thus storing the most significant bits.

(7) The 12 output pins of the A/D are put in the high *Z* state.



(a)

```
(K)*=Ø2ØØ

Ø2ØØ A9 LDA #FF
Ø2Ø2 8D STA AØØ2
Ø2Ø5 A9 LDA #8F
Ø2Ø7 8D STA AØØ3
Ø2ØA A9 LDA #CØ
Ø2ØC 8D STA AØØC
Ø2ØF A5 LDA ØC
Ø211 8D STA AØØØ
Ø214 A5 LDA ØD
Ø216 29 AND #87
Ø218 8D STA AØØ1
Ø21B A9 LDA #EØ
Ø21D 8D STA AØØC
```

(b)

Fig. 6. (a) D/A conversion subroutine flow chart and (b) D/A conversion subroutine listing.

3.2. The digital-to-analogue conversion subroutine

The sequence of operations necessary for D/A conversion is summarized in the flow chart shown in Fig. 6(a); the corresponding subroutine is shown in Fig. 6(b). The sequence of instructions is as follows.

(1) Port B is made into an output, and PA0, PA1, PA2 and PA7 are also made into outputs.

(2) CB2 is set to zero volts.

(3) The least significant bits are transferred from memory to the output register B.

(4) Bits 3, 4, 5 and 6 of the memory byte containing the most significant bits are masked; since this operation makes PA3 go low it also ensures that the D/A converter is in the high Z state.

(5) After the masking operation, the most significant bits are transferred to the output register A.

(6) The data word is latched and conversion is initiated; CB2 goes high.

4. Conclusion

The assembly language subroutines described can be easily integrated into larger assembly language programs for those applications requiring machine speed execution. Moreover, they may also be easily incorporated in BASIC (interpreted) programs for those applications where this is suitable.

This interface is used in our research on the control of robot manipulators. After many months of use, the interface has proved reliable and stable (no drift, no changes of gain etc.). We are at present equipping our servo system laboratory with ten of these interfaces.

It should be noted that no demultiplexing and sample-and-hold circuitry necessary for multivariable controls was included on the D/A card, thus reducing costs and complexity. We are at present developing such circuitry on a separate card for controlling small multivariable systems.

Acknowledgments

The work reported in this paper has been carried out with the help of our technicians R. Grenier and Y. Léonard.

References

1 R. K. Forcé, J. Boyd and E. Harris, Design of a multiplexed eight channel analog input 12-bit analog-to-digital converter interfaced to a Commodore PET 8-bit microcomputer, *Interfaces Comput.*, *1* (1982) 59 - 62.
2 *Data Acquisition Products Catalog Supplement*, Analog Devices, Norwood, 1979.
3 *Linear Integrated Circuits*, National Semiconductor, Santa Clara, CA, 1973.
4 *Product Data Book*, Burr-Brown, Tucson, AZ, 1982.
5 *AIM-65 Microcomputer User's Guide*, Rockwell International, Anaheim, CA, 1978.